IDEC Chip Design Contest

An Energy-Efficient 16-Channel Charge Trackable Inductor-Based Stimulation System

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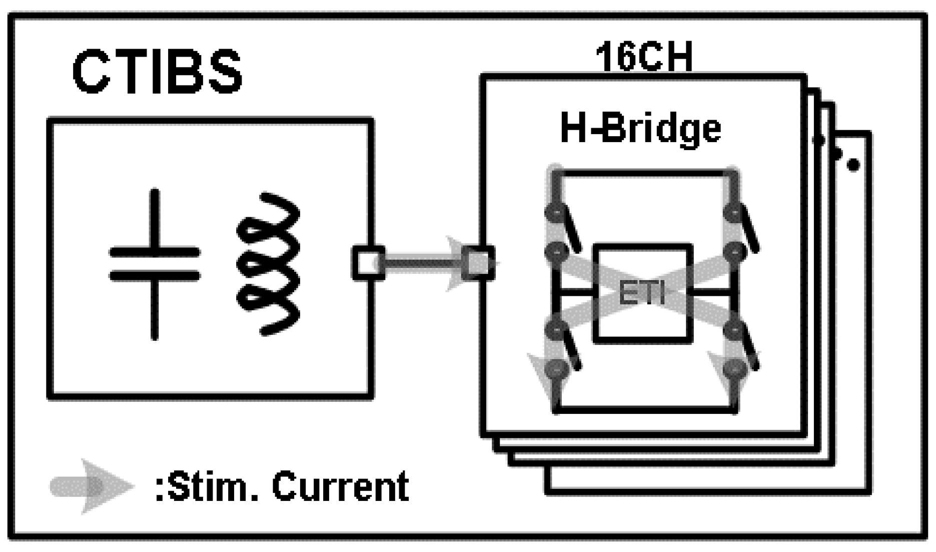
Abstract

These days, the concept of ”electroceuticals” is emerging that maximizes the effectiveness of treatment by applying electrical stimulation only to the desired area but minimizes side effects. In order to realize electroceuticals, stimulators that can be inserted into the body must be developed. The requirements are such as enhancing power efficiency, securing safety, and effective electrical stimulation. Therefore, the stimulator must operate energy efficiently and must be able to track the amount of stimulation charges delivered to the target cell. However, there is a problem that the existing electrical stimulator does not satisfy the above requirements. Therefore, this study developed Charge Trackable Inductor-Based Stimulator (CTIBS), which operates in 80% of peak stimulator efficiency, and its charge error between anodic and cathodic stimulation to be less than 1.36%. In addition, the stimulation channels are expanded to 16-channels so that stimulation area and density can be freely controlled. The IC chip was designed in RF 180nm process, taking up the area of 5mm^2

Design

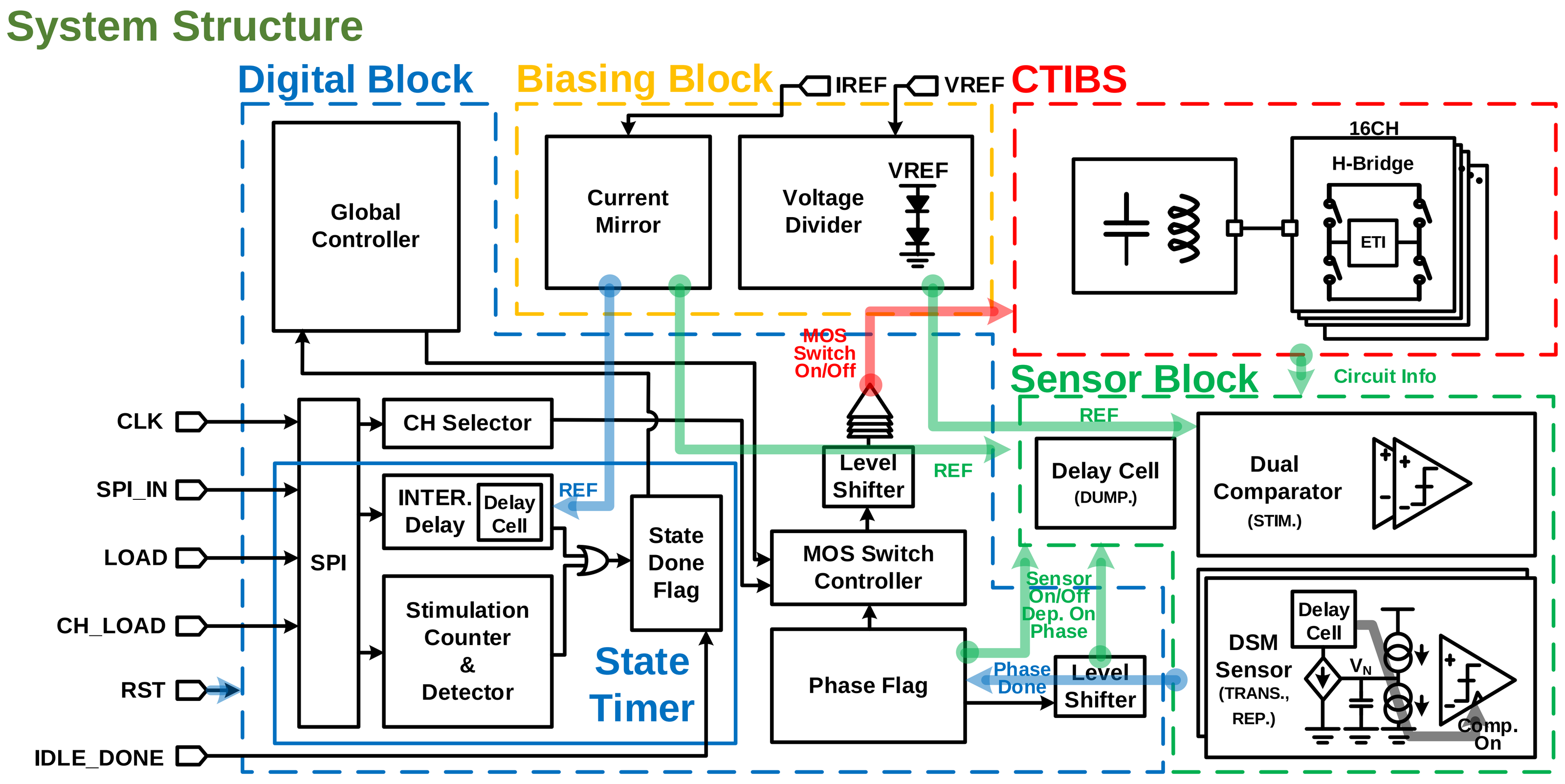
Charge Trackable Inductor-Based Stimulator (CTIBS)



CTIBS consists of a stimulation capacitor, inductor, MOS switches. It is directly connected to 16 H-bridge stimulation channels with the electrode-tissue model (ETI). The MOS switches are controlled by commands transmitted from the digital circuit and the sensor block according to the four states of the system and the four phases of the stimulation state.

In CTIBS, the stimulation capacitor measures the amount of stimulation charge, enabling charge tracking and balance. The inductor returns the excess energy remaining in the stimulation circuit to the supply so that the stimulation circuit works in an energy-efficient way.

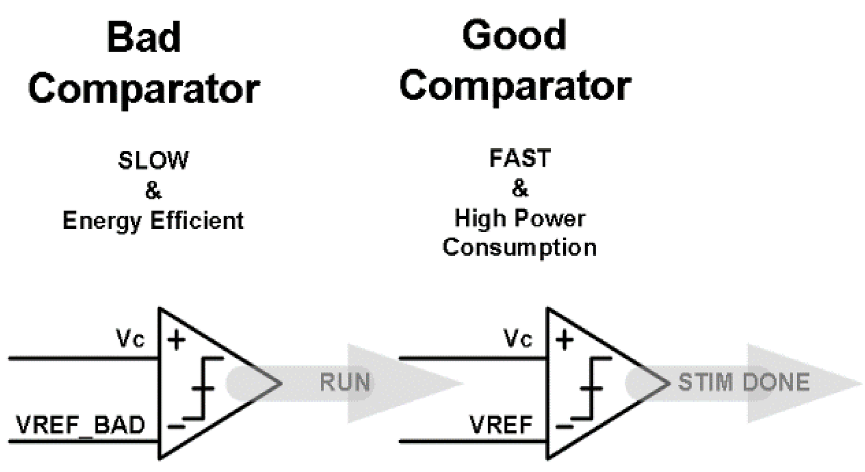
The Entire System Structure



The system is largely divided into a digital block, a biasing block, a sensor block, and a stimulation circuit.

These four blocks proceed with 4 states and 4 stimulation phases through interaction. The four states consist of an idle state (IDLE), an intermediate delay state (INTER), and cathodic/anodic stimulation state (CAT/AN_STIM). Each stimulation state consists of four phases, which grants energy-efficiency and charge tracking ability to the proposed stimulator. The four phases consist of stimulation phase (STIM), transfer phase (TRAN), replenishing phase (REP), and dump phase (DUMP).

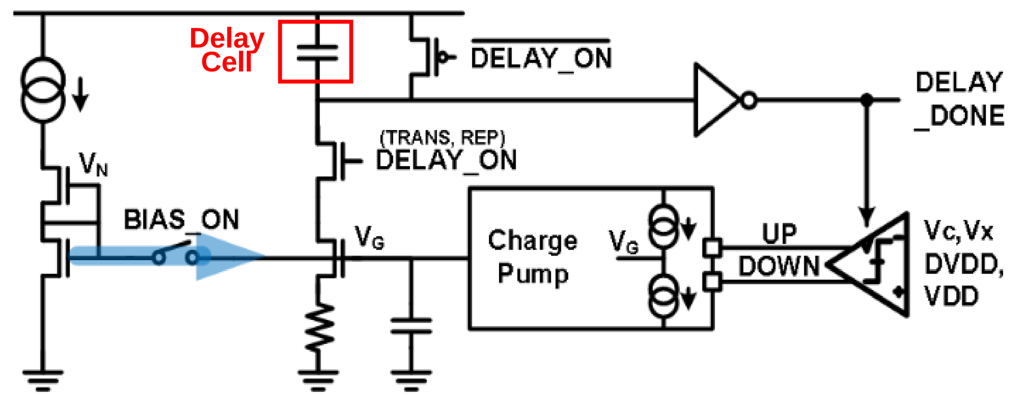
Double Comparator Phase Control



As the STIM phase is repeated, the charge accumulates in the double layer capacitor of the electrode. This changes the amplitude of the stimulation current, thus the duration taken to bring/send the same amount of charge changes significantly as time goes by. Therefore, a comparator that can make an accurate judgment regardless of the varying duration is needed.

To solve the problem, the series of two comparators were used. The first one operates in slow speed but consumes low energy. This was realized by a self-clocked dynamic comparator, whose clock speed depends on the voltage level of sensing point. The other operates in fast speed but consumes lots of energy, which was realized by a continuous comparator. Using these two comparators, it was able to make a comparator that works accurately and energy-efficiently.

ΔΣ Delay Cell Modulation (DSM) Sensor Phase Control



The duration of TRANS and REP do not change significantly even after several repeated cycles. Thus, the ΔΣ delay cell was used which saves the duration time and adjusts it by a charge pump. This operates energy-efficiently, because the comparator judges only once during the phase.

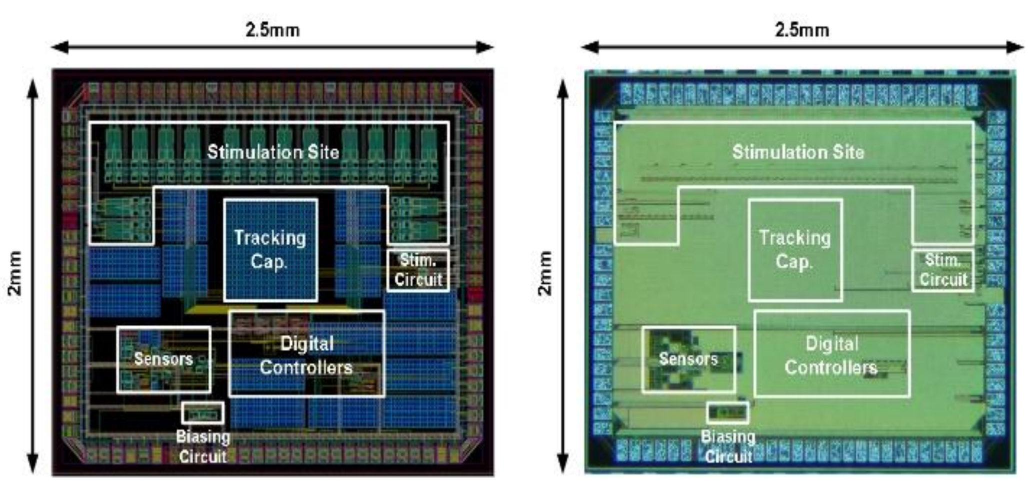
During DELAY_ON, either when it is TRANS or REP phase signal is on, the dependent current source charges the capacitor, a delay cell. When the capacitor voltage exceeds the threshold of the inverter, the DELAY_ON signal is turned off, discharging the capacitor, and moving to the next phase.

The charge pump adjusts the current level of dependent current source. According to the information transmitted from the comparator, it increases or decreases V_G. For the fast determination of the duration, digital logic was implemented, which integrates the error information in the flip-flop cell.

A degenerative resistor is placed at the source terminal of the dependent current source, increasing the linearity of the current change according to V_G.

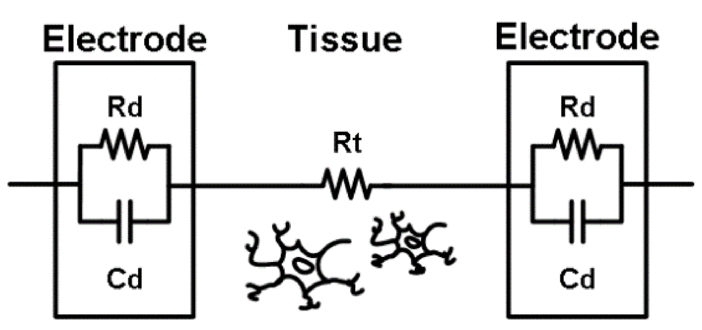
Result & Conclusion

Chip Layout



The integrated circuit is designed with a TSMC 180nm RF CMOS process. The size is 2.5mm x 2mm, an area of 5 ㎟.

Electrode-tissue Interference Model

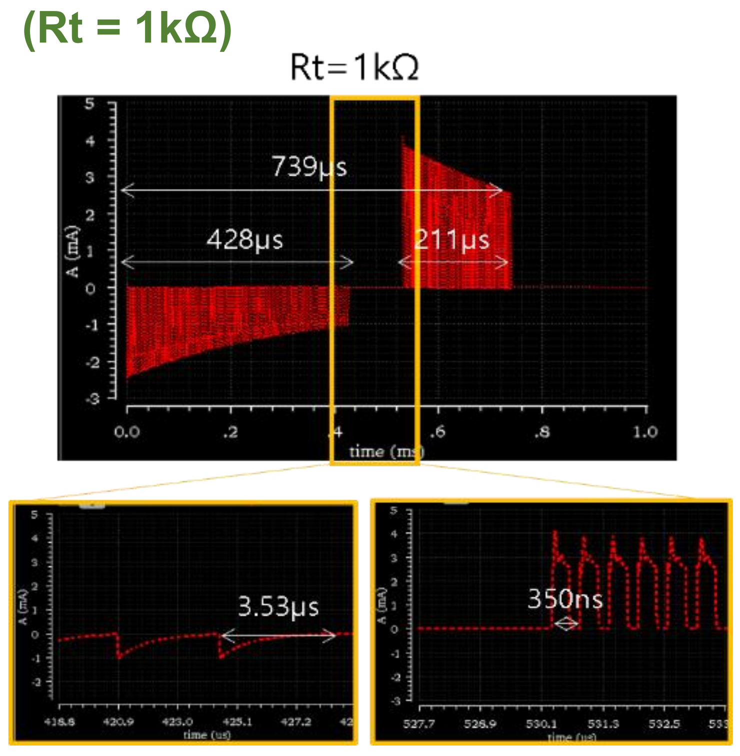


Rt=500Ω, 1kΩ, 5kΩ, Rd=10MΩ, and Cd=500nF

Result

The following results are simulated by ADE tool from Cadence. The PCB experiment was failed due to an error in the initial stage of the chip.

• Waveform of stimulation current (Rt = 1kΩ)



• Charge Tracking Error

R_t	Target Charge	Delivered Charge	Error
500Ω		318.12nC	6.04%
1kΩ	300nC	316.66nC	5.55%
5kΩ		315.28nC	4.85%

• Charge Balancing Error

R_t	CS	AS	Residuals				Error	
			B/F Passive		A/F Passive		B/F Passive	A/F Passive
			Charge	Voltage	Charge	Voltage		
500Ω	318.12nC	319.06nC	944pC	3.76mV	4.10fC	16.4nV	0.29%	0%
1kΩ	316.66nC	314.80nC	1.86nC	7.26mV	86.3aC	345pV	0.59%	0%
5kΩ	315.28nC	310.95nC	4.28nC	17.1mV	12.2pC	48.6uV	1.36%	0%

• Stimulation Efficiency

R_t		
500Ω	1kΩ	5kΩ
1.073μJ/1.273μJ → 84.3%	1.101μJ/1.280μJ → 86.0%	1.114μJ/1.278μJ → 87.2%

• Stimulator Efficiency

R_t		
500Ω	1kΩ	5kΩ
1.073μJ/1.340μJ → 80.1%	1.101μJ/1.384μJ → 79.6%	1.114μJ/1.665μJ → 66.9%

Acknowledgement

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